Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A semiconductor device comprising one or two semiconductor chips, each of said semiconductor chips including an input circuit and an input pad, said input circuit comprising:

a wiring for connecting said input pad to an inner circuit;

a first electrostatic protection element electrically connected to said wiring;

a second electrostatic protection element provided in vicinity of said wiring; and

a fuse provided between said wiring and said second electrostatic protection element, wherein

when said semiconductor device has said one semiconductor chip, said wiring and said second electrostatic protection element are connected to each other through said fuse, and

when said semiconductor device has said two semiconductor chips, said fuse of each of said input circuits is disconnected so that said second electrostatic protection element of each of said input circuits is electrically disconnected from said wiring of each of said input circuits.

2. (currently amended) A semiconductor device comprising one or two semiconductor chips, each of said semiconductor chips including an input circuit and an input pad, said input circuit comprising:

a wiring for connecting said input pad to an inner circuit;

first and second electrostatic protection elements provided in vicinity of said wiring; and

first and second fuses provided between said wiring and said first and second electrostatic protection elements, respectively, wherein

when said semiconductor device has said one semiconductor chip, said wiring and said first and second electrostatic protection elements are connected to each other through said first and second fuses, and

when said semiconductor device has said two semiconductor chips, said first or second fuse of each of said input circuits is disconnected so that said first or second electrostatic protection element of each of said input circuits is electrically disconnected from said wiring of each of said input circuits.

3. (currently amended) A semiconductor device comprising one semiconductor chip or semiconductor chips in a number of n, said one semiconductor chip or each of said semiconductor chips in the number of n including an input circuit and an input pad, said input circuit comprising:

a wiring for connecting said input pad to an inner circuit;

a first electrostatic protection element electrically connected to said wiring;

second to n-th electrostatic protection elements provided in vicinity of said wiring; and

second to n-th fuses provided between said wiring and said second to n-th electrostatic protection elements, respectively, wherein

when said semiconductor device has said one semiconductor chip, said wiring and said second to n-th electrostatic protection elements are connected to each other through said second to n-th fuses, and

when said semiconductor device has said semiconductor chips in the number of n, said second to n-th fuses of each of said

input circuits are disconnected so that said second to n-th electrostatic protection elements of each of said input circuits are electrically disconnected from said wiring of each of said input circuits, wherein said n is an integer more than two.

4. (currently amended) A semiconductor device comprising one semiconductor chip or semiconductor chips in a number of n, said one semiconductor chip or each of said semiconductor chips in the number of n including an input circuit and an input pad, said input circuit comprising:

a wiring for connecting said input pad to an inner circuit;

first ~~and~~ to n-th electrostatic protection elements provided in vicinity of said wiring; and

first ~~and~~ to n-th fuses provided between said wiring and said first and n-th electrostatic protection elements, respectively, wherein

when said semiconductor device has said one semiconductor chip, said wiring and said first to n-th electrostatic protection elements are connected to each other through said first to n-th fuses, and

when said semiconductor device has said semiconductor chips in the number of n, ~~said~~ second to said n-th fuses of each of said input circuits are disconnected so that said first electrostatic protection element of each of said input circuits is electrically connected to and ~~said~~ second to said n-th electrostatic protection elements of each of said input circuits are electrically disconnected from said wiring of each of said input circuits, wherein said n is an integer more than two.

5. (currently amended) A semiconductor device comprising one semiconductor chip or a plurality of semiconductor chips, said one semiconductor chip or each of the plurality of said

semiconductor chips including an input circuit and an input pad, said input circuit comprising:

a wiring for connecting said input pad to an inner circuit;

a plurality of electrostatic protection elements provided in vicinity of said wiring; and

a plurality of fuses one each provided between said wiring and the plurality of said electrostatic protection elements, respectively, wherein

when said semiconductor device has said one semiconductor chip, said wiring and ~~all~~ the plurality of said electrostatic protection elements are connected to each other through the plurality of said fuses, and

when said semiconductor device has said plurality of said semiconductor chips, a predetermined number of the plurality of said fuses of each of said input circuits are disconnected so that a part of the plurality of said electrostatic protection elements of each of said input circuits corresponding to the predetermined number of the plurality of said ~~disconnected~~ fuses are electrically disconnected from said wiring of each of said input circuits.

6. (currently amended) A semiconductor device comprising one semiconductor chip or semiconductor chips in a number of o or p, said one semiconductor chip or each of said semiconductor chips in the number of o or p including an input circuit and an input pad, said input circuit comprising:

a wiring for connecting said input pad to an inner circuit;

a first electrostatic protection element electrically connected to said wiring;

second to m-th electrostatic protection elements provided in vicinity of said wiring; and

second to m-th fuses provided between said wiring and said second to m-th electrostatic protection elements, respectively, wherein

when said semiconductor device has said one semiconductor chip, said wiring and said first and said second to m-th electrostatic protection elements are connected to each other, and

when said semiconductor device has said semiconductor chips in the number of o, ~~a first predetermined fuses of~~ (m/o + 1)-th to said m-th fuses of each of said input circuits are disconnected so that said first and said second to (m/o)-th electrostatic protection elements of each of said input circuits are electrically connected to and ~~said (m/o + 1)th~~ (m/o + 1)-th to said m-th electrostatic protection elements of each of said input circuits are disconnected from said wiring of each of said input circuits,

when said semiconductor device has said semiconductor chips in the number of p, ~~a second predetermined fuses of~~ (m/p + 1)-th to said m-th fuses of each of said input circuits are disconnected so that said first and second to (m/p)-th electrostatic protection elements of each of said input circuits are electrically connected to and ~~said (m/p + 1)th~~ (m/p + 1)-th to said m-th electrostatic protection elements of each of said input circuits are disconnected from said wiring of each of said input circuits, wherein said o and p are integers more than 2 and said m is the lowest common multiple of said o and p.

7. (currently amended) A semiconductor device comprising one semiconductor chip or semiconductor chips in a number of o or p, said one semiconductor chip or each of said semiconductor chips in the number of o or p including an input circuit and an input pad, said input circuit comprising:

a wiring for connecting said input pad to an inner circuit;

first to m-th electrostatic protection elements provided in vicinity of said wiring; and

first to m-th fuses provided between said wiring and said first to m-th electrostatic protection elements, respectively, wherein

when said semiconductor device has said one semiconductor chip, said wiring and said first to m-th electrostatic protection elements are connected to each other through said first to m-th fuses, and

when said semiconductor device has said semiconductor chips in the number of o, ~~a first predetermined fuses of~~ (m/o + 1)-th to said m-th fuses of each of said input circuits are disconnected so that said first to (m/o)-th electrostatic protection elements of each of said input circuits are electrically connected to and ~~said (m/o + 1)th~~ (m/o + 1)-th to said m-th electrostatic protection elements of each of said input circuits are disconnected from said wiring of each of said input circuits,

when said semiconductor device has said semiconductor chips in the number of p, ~~a second predetermined fuses of~~ (m/p + 1)-th to said m-th fuses of each of said input circuits are disconnected so that said first to (m/p)-th electrostatic protection elements of each of said input circuits are electrically connected to and ~~said (m/p + 1)th~~ (m/p + 1)-th to said m-th electrostatic protection elements of each of said input circuits are disconnected from said wiring of each of said input circuits, wherein said o and p are integers more than 2 and said m is the lowest common multiple of said o and p.

8. (currently amended) A semiconductor device comprising one semiconductor chip or semiconductor chips in a number of o, p,

or q, said one semiconductor chip or each of said semiconductor chips in the number of o, p, or q including an input circuit and an input pad, said input circuit comprising:

a wiring for connecting said input pad to an inner circuit;

a first electrostatic protection element electrically connected to said wiring;

second to m-th electrostatic protection elements provided in vicinity of said wiring; and

second to m-th fuses provided between said wiring and said second to m-th electrostatic protection elements, respectively, wherein

when said semiconductor device has said one semiconductor chip, said wiring and said first and said second to m-th electrostatic protection elements are connected to each other, and

when said semiconductor device has said semiconductor chips in the number of o, ~~a first predetermined fuses of~~ (m/o + 1)-th to said m-th fuses of each of said input circuits are disconnected so that said first and second to (m/o)-th electrostatic protection elements of each of said input circuits are electrically connected to and ~~said (m/o + 1)th~~ (m/o + 1)-th to said m-th electrostatic protection elements of each of said input circuits are disconnected from said wiring of each of said input circuits,

when said semiconductor device has said semiconductor chips in the number of p, ~~a second predetermined fuses of~~ (m/p + 1)-th to said m-th fuses of each of said input circuits are disconnected so that said first and second to (m/p)-th electrostatic protection elements of each of said input circuits are electrically connected to and ~~said (m/p + 1)th~~ (m/p + 1)-th to said m-th electrostatic protection elements of each of said input circuits are disconnected from said wiring of each of said input circuits,

when said semiconductor device has said semiconductor chips in the number of q, ~~a third predetermined fuses of~~ (m/q + 1)-th to said m-th fuses of each of said input circuits are disconnected so that said first and second to (m/q)-th electrostatic protection elements of each of said input circuits are electrically connected to and ~~said (m/q + 1)th~~ (m/q + 1)-th to said m-th electrostatic protection elements of each of said input circuits are disconnected from said wiring of each of said input circuits, wherein said o, p, and q are integers more than 2 and said m is the lowest common multiple of said o, p, and q.

9. (currently amended) A semiconductor device comprising one semiconductor chip or semiconductor chips in a number of o, p, or q, said one semiconductor chip or each of said semiconductor chips in the number of o, p, or q, including an input circuit and an input pad, said input circuit comprising:

a wiring for connecting said input pad to an inner circuit;

first to m-th electrostatic protection elements provided in vicinity of said wiring; and

first to m-th fuses provided between said wiring and said first to m-th electrostatic protection elements, respectively, wherein

when said semiconductor device has said one semiconductor chip, said wiring and said first to m-th electrostatic protection elements are connected to each other through said first to m-th fuses, and

when said semiconductor device has said semiconductor chips in the number of o, ~~a first predetermined fuses of~~ (m/o + 1)-th to said m-th fuses of each of said input circuits are disconnected so that said first to (m/o)-th electrostatic protection elements of each of said input circuits are electrically connected to and ~~said (m/o + 1)th~~ (m/o + 1)-th to said m-th electrostatic protection elements of each of said

input circuits are disconnected from said wiring of each of said input circuits,

when said semiconductor device has said semiconductor chips in the number of p, ~~a second predetermined fuses of~~ (m/p + 1)-th to said m-th fuses of each of said input circuits are disconnected so that said first to (m/p)-th electrostatic protection elements of each of said input circuits are electrically connected to and ~~said (m/p + 1)th~~ (m/p + 1)-th to said m-th electrostatic protection elements of each of said input circuits are disconnected from said wiring of each of said input circuits,

when said semiconductor device has said semiconductor chips in the number of q, ~~a third predetermined fuses of~~ (m/q + 1)-th to said m-th fuses of each of said input circuits are disconnected so that said first to (m/q)-th electrostatic protection elements of each of said input circuits are electrically connected to and ~~said (m/q + 1)th~~ (m/q + 1)-th to said m-th electrostatic protection elements of each of said input circuits are disconnected from said wiring of each of said input circuits, wherein said o, p, and q are integers more than 2 and said m is the lowest common multiple of said o, p, and q.

10. (currently amended) The semiconductor device according to claim 1, wherein said first and second electrostatic protection elements of each of said input circuits are capacitors formed by MOS transistors.

11. (currently amended) The semiconductor device according to claim 2, wherein said first and second electrostatic protection elements of each of said input circuits are capacitors formed by MOS transistors.

12. (currently amended) The semiconductor device according to claim 3, wherein said first and second to n-th electrostatic protection elements of each of said input circuits are capacitors formed by MOS transistors.

13. (currently amended) The semiconductor device according to claim 4, wherein said first to n-th electrostatic protection elements of each of said input circuits are capacitors formed by MOS transistors.

14. (currently amended) The semiconductor device according to claim 5, wherein said plurality of said electrostatic protection elements of each of said input circuits are capacitors formed by MOS transistors.

15. (currently amended) The semiconductor device according to claim 6, wherein said first and second to m-th electrostatic protection elements of each of said input circuits are capacitors formed by MOS transistors.

16. (currently amended) The semiconductor device according to claim 7, wherein said first to m-th electrostatic protection elements of each of said input circuits are capacitors formed by MOS transistors.

17. (currently amended) The semiconductor device according to claim 8, wherein said first and second to m-th electrostatic protection elements of each of said input circuits are capacitors formed by MOS transistors.

18. (currently amended) The semiconductor device according to claim 9, wherein said first to m-th electrostatic protection

elements of each of said input circuits are capacitors formed by MOS transistors.

19-43. (canceled)